# A High Efficiency Topology for 12V VRM — Push-Pull Buck and Its Integrated Magnetics Implementations

Jia Wei, Peng Xu and Fred C. Lee

Center for Power Electronics Systems
The Bradley Department of Electrical and Computer Engineering
Virginia Polytechnic Institute and State University
Blacksburg, VA 24061 USA

*Abstract* — **As the computer processors moving forward quickly, their power management becomes more and more challenging. Nowadays, for the desktop and workstation applications, VRM input voltage has moved to the 12V output of the silver box. The state of the art 12V VRM topology is buck. Because of the extreme duty-cycle, buck has a lot of limitations however. This paper presents a high efficiency, fast transient response topology for the 12V VRM application — Push-Pull Buck (PPB). The Push-Pull Buck has significantly better performance over buck converter. A few integrated magnetics implementations are discussed and tested. Experimental results confirm the theoretical prediction.**

## I. Introduction

The computer industry has been quickly expanding since the early 80's. Processors are becoming faster and more powerful. Accordingly, their power consumption increases dramatically. An evolution began when the high-performance Pentium processor was driven by a non-standard, less than 5V power supply, instead of drawing its power from the 5V plane on the system board. In order to provide the power as fast as possible, a so-called VRM, Voltage Regulator Module, is put close to the processor. In the past, VRMs basically drew power from the 5V output of the silver box. Nowadays, for the desktop and workstation applications, VRM input voltage has moved to the 12V output of the silver box. And for server applications, the 48V VRM will emerge as a standard practice.

VRM design has a very fast moving target associated with the fast development of processors. Fig.1 is the Intel roadmap of voltage and current of the CPU load for VRMs [1]. Future microprocessors will run at very low voltage (below 1V), high current consumption of up to 100 A, and fast dynamics of about 400A/us. These requirements introduce great challenges in VRM design.

Today's 12V VRMs use the multi-phase interleaving synchronous buck topology [2][3][4][5][6]. Due to the very low output voltage, the buck converter has very small duty-cycle, which can be even smaller than 0.1 in the future. This extreme duty-cycle impairs the VRM's efficiency and poses obstacles for transient response. Also the extreme duty-cycle makes the top switch current sensing difficult and may even cause malfunction at high switching frequency due to the very short conduction time for the top switch.

This paper presents a novel Push-Pull Buck (PPB) converter as a candidate of the 12V VRMs. With properly designed turns ratio, this circuit has favorable duty-cycle, which provides an opportunity to improve both the efficiency and the transient response. This circuit also involves in the output inductors as current-doubler inductors, therefore the already developed techniques on the current-doublers are all applicable, including integrated magnetics, built-in filter, and coupled current-doubler techniques.

Four 12V input, 1.5V/50A output VRM prototypes were built to test the performances of different implementations. Each prototype employs four-phase interleaving technique to achieve ripple cancellation to minimize the filter size and improve the transient response. For comparison, a four-phase interleaving synchronous buck VRM prototype was also built with everything but the topology same. The experimental result shows the proposed Push-Pull Buck VRM achieves 6% efficiency improvement over the synchronous buck VRM.

## II. Limitations of Today's Approach

Multi-phase interleaving synchronous buck topology, as shown in Fig.2, is widely used in the 12V VRMs. Interleaving is to parallel a few modules, and to phase-shift their drive signals. The major benefits are output ripple cancellation and the improved transient response. In addition, better thermal management and package flexibility are also present.

Multi-phase interleaving doesn't change the DC voltage gain from each single module. So the multi-phase interleaving buck has a voltage gain as

* This work was supported primarily by Intel, Texas Instruments, National Semiconductors, Intersil, TDK, Hitachi, Hipro, Power-One, and Delta Electronics.

Also, this work made use of ERC shared facilities supported by the National Science Foundation Under Award Number EEC-9731677

0-7803-7404-5/02/$17.00 (c) 2002 IEEE

grounds. The above steps are illustrated in Fig.6. Then redraw the configuration, the proposed so-called Push-Pull Buck (PPB) is shown in Fig.7. Fig.8 is the operation principle of the Push-Pull Buck.

It is understandable that the Push-Pull Buck has similar basic operation waveforms to the Push-Pull Forward converter's. Hence in this paper, the circuit operation principle will not be discussed in detail.

But there is still some difference between the Push-Pull Buck and the Push-Pull Forward.

For Push-Pull Buck, the voltage conversion gain is

$$V_o/V_{in} = D/(D+n)$$

while for the Push-Pull Forward, the voltage conversion gain is

$$V_o/V_{in} = D/n$$

Symmetrical transient response is preferred for transient design [9][10]. For 12V input, 1.5V output, the turns ratio is normally "2:1" to yield symmetrical transient response. With 2:1 turns ratio, the steady state duty-cycle is 0.25 for Push-Pull Forward and 0.285 for the Push-Pull Buck.

In hard-switching 12V VRMs, the dominant losses are the top switch turn-off loss and the bottom switch conduction loss [9]. Compare the switch current waveforms, shown in Fig.9, it is observed that the Push-Pull Buck has smaller top switch turn-off current and smaller bottom switch rms current than the Push-Pull Forward converter, which means higher efficiency can be expected. The intuition is because the Push-Pull Buck delivers the transformer primary side current directly to the output in addition to the secondary current. This is a more effective way than the way Push-Pull Forward does.

With the extended duty-cycle, compared with Synchronous Buck, the top switch turn-off current is much smaller for Push-Pull Buck. This reduces the turn-off loss dramatically. However, Push-Pull Buck has a little larger bottom switch rms current. Fig.10 is the device loss estimation of buck and Push-Pull Buck. From the chart, it is seen that, for Push-Puck, the reduced turn-off loss is more than enough to compensate the increased conduction. Moreover, the top switch conduction loss is also smaller. Therefore Push-Pull Buck is expected to have higher efficiency than Buck.

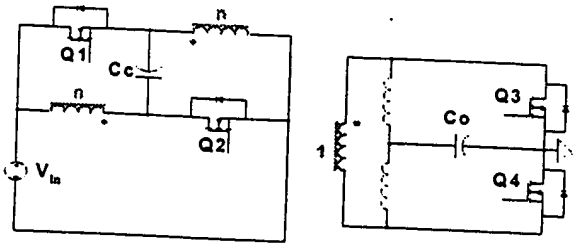


Fig.5 Push-Pull Forward converter

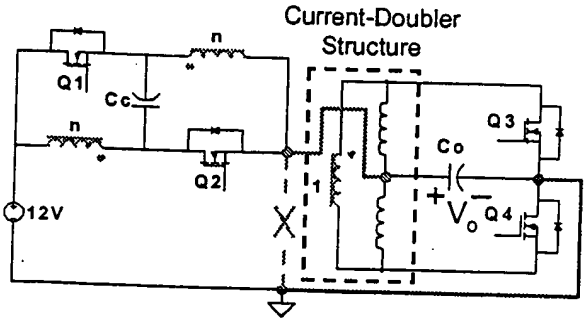


Fig.6 Derive the Push-pull Buck from Push-pull Forward

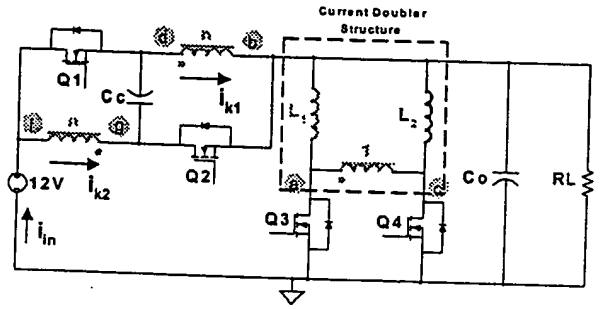


Fig.7 Push-Pull Buck converter

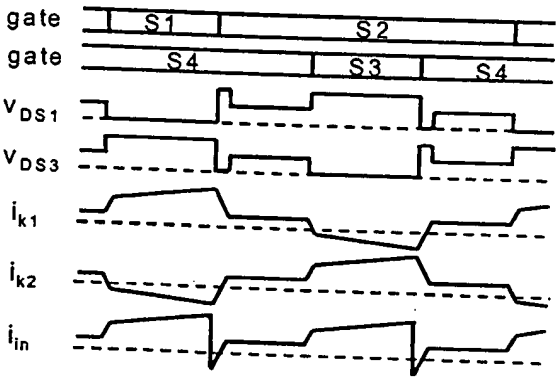


Fig.8 Operation waveforms of the Push-Pull buck converter

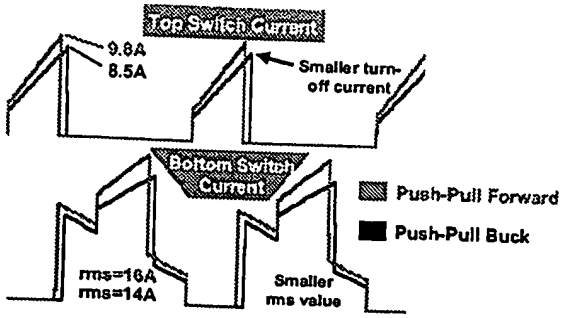


Fig.9 Switch current comparison of Push-Pull Forward and Push-Pull Buck
Vin=12V Vo=1.5V, Io=50A, n=2
L=300nH/phase, Fs=300KHz/phase, 4 phases

## IV. Experimental Results

For each IM implementation, a four-phase interleaving 1.5V/50A prototype was built. Fig.13 shows the IM-4 prototype. For comparison, a four-phase interleaving buck is also built with everything except the topology same. MOSFET Si4884DY ($R_{dson}$ = 10 mΩ, $Q_g$ = 15.3 nC) is used as the top switches; Si4874DY ($R_{dson}$ = 7 mΩ, $Q_g$ = 35 nC) is used as the bottom switches. No devices are paralleled.

Design specs are $V_{in}$=12V, $V_o$=1.5V, Max Load=50A, $F_s$=300KHz/phase, L=300nH/phase (four-phase interleaving). Philips EI-18 planar cores and PCB windings are employed to build the inductor. Fig.14 shows the winding arrangement. Noting the output inductor windings are paralleled. The air gap is on the center leg only. In each circuit, the output cap is 6×1200μF OSCON plus 18×22μF ceramic.

Fig.15~16 are its experimental waveforms, noting the current scale is 5A/div. $I_{in}$ was got without any additional input filter. In Fig.17 are four phase top switch currents. It is observed that good current sharing is achieved. Experimental efficiency comparison is shown in Fig.18. As predicted, IM-4 has the highest efficiency, with 6% improvement over buck converter. Fig.19~21 are the output voltage waveforms at load transient between 0A and 50A.

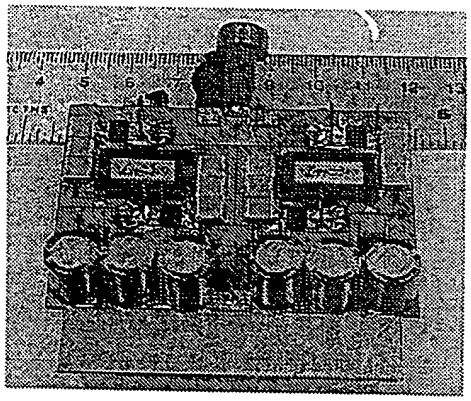

Fig.13 Prototype picture of the IM-4 Push-Pull Buck

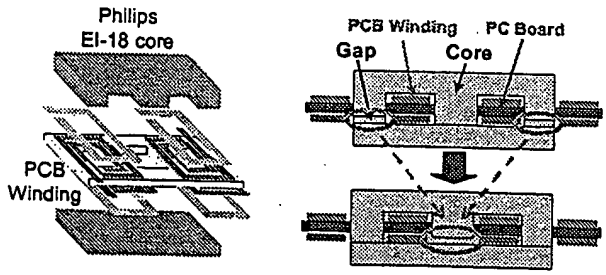


Fig.14 Winding arrangement of the IM-4 Push-Pull Buck

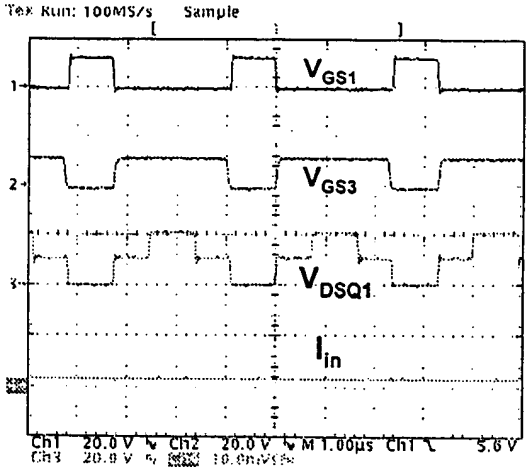


Fig.15 Test waveforms @ 5A load

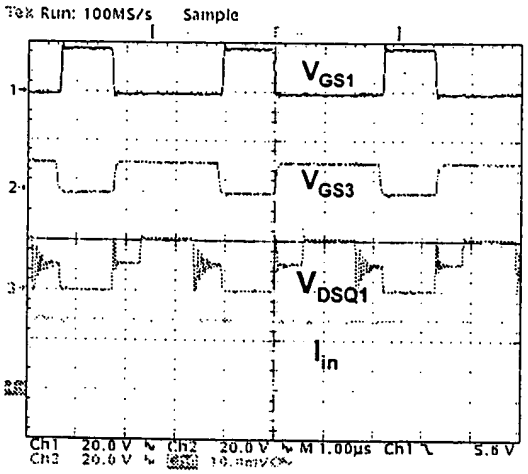


Fig.16 Test waveforms @ 50A load

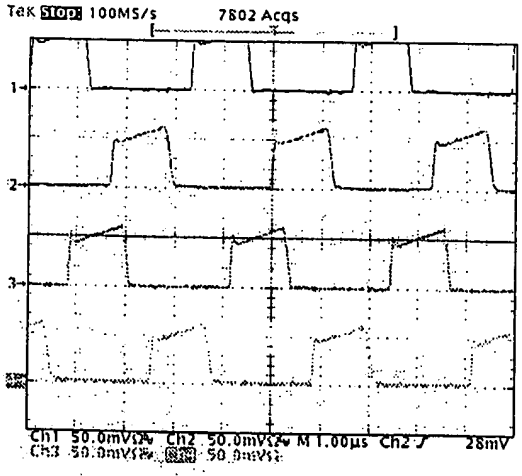


Fig.17 Top switch currents